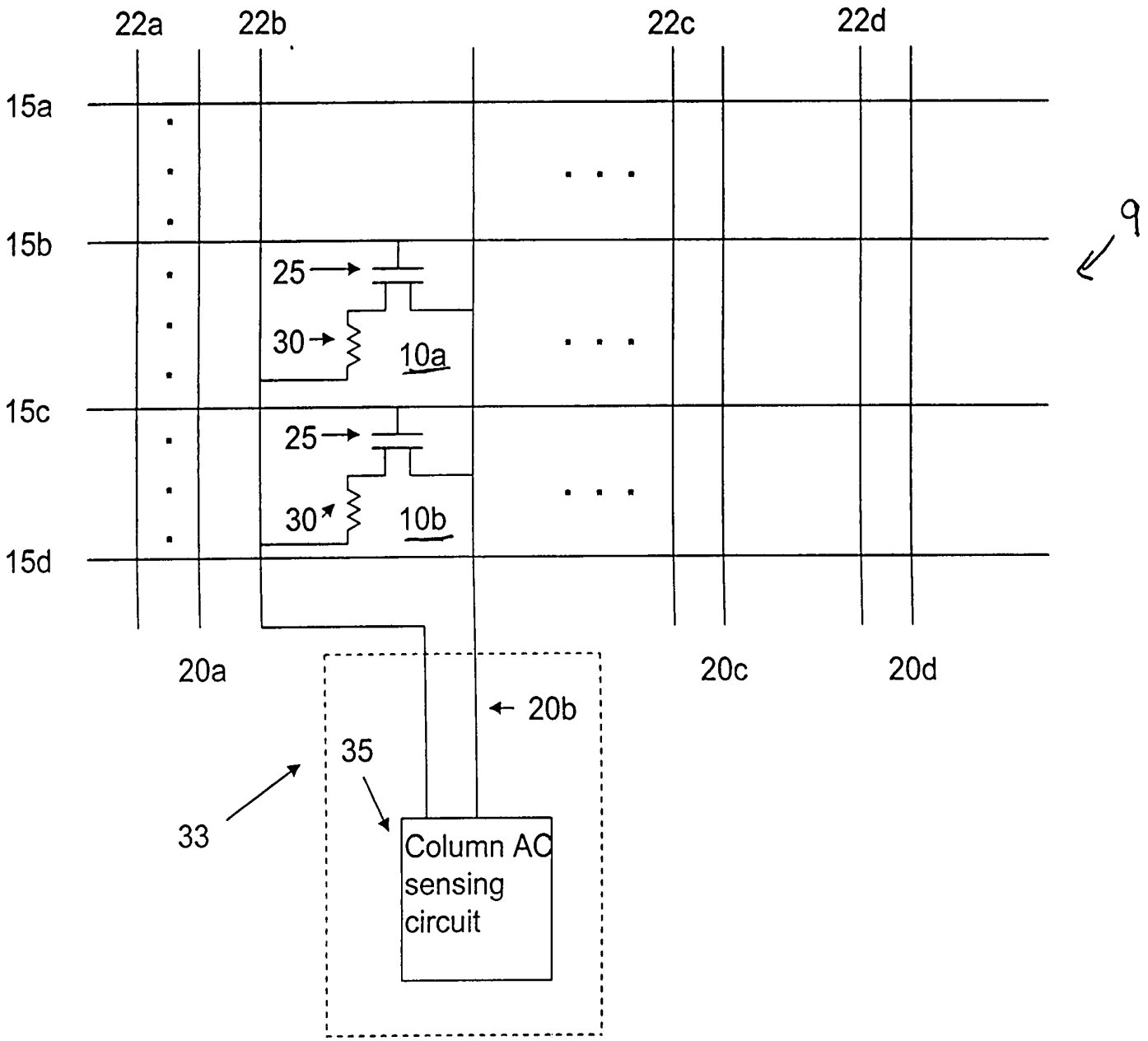

22a
22b
22c
22d
15a
15b
15c
15d
25
30
10a
25
30
10b
9
20a
20c
20d
20b
35
33
Column AC sensing circuit

Fig. 1

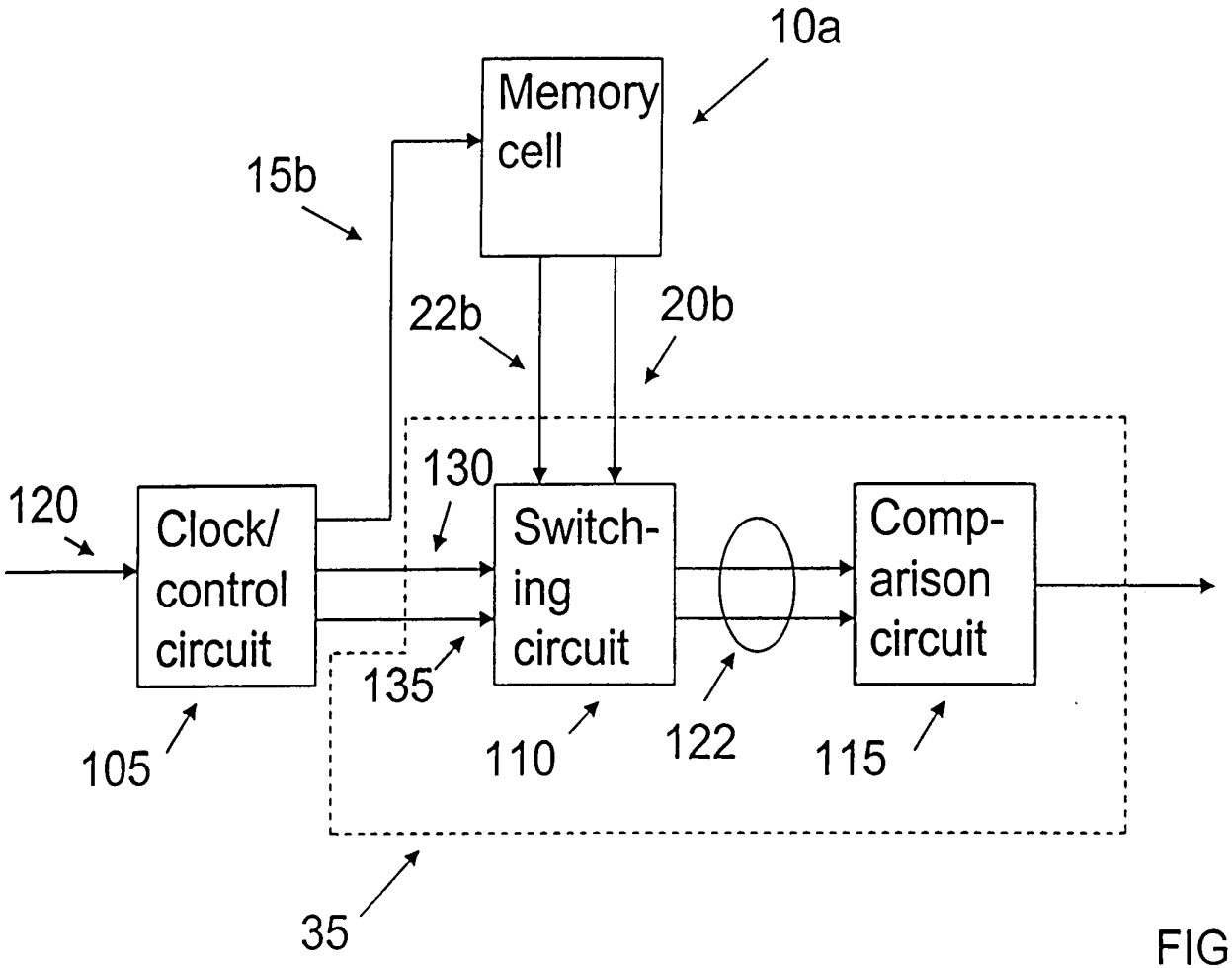

10a
Memory cell
8
15b
22b
20b
130
120
Clock/ control circuit
Switch- ing circuit
Comp- arison circuit
135
105
110
122
115
35

FIG. 2A

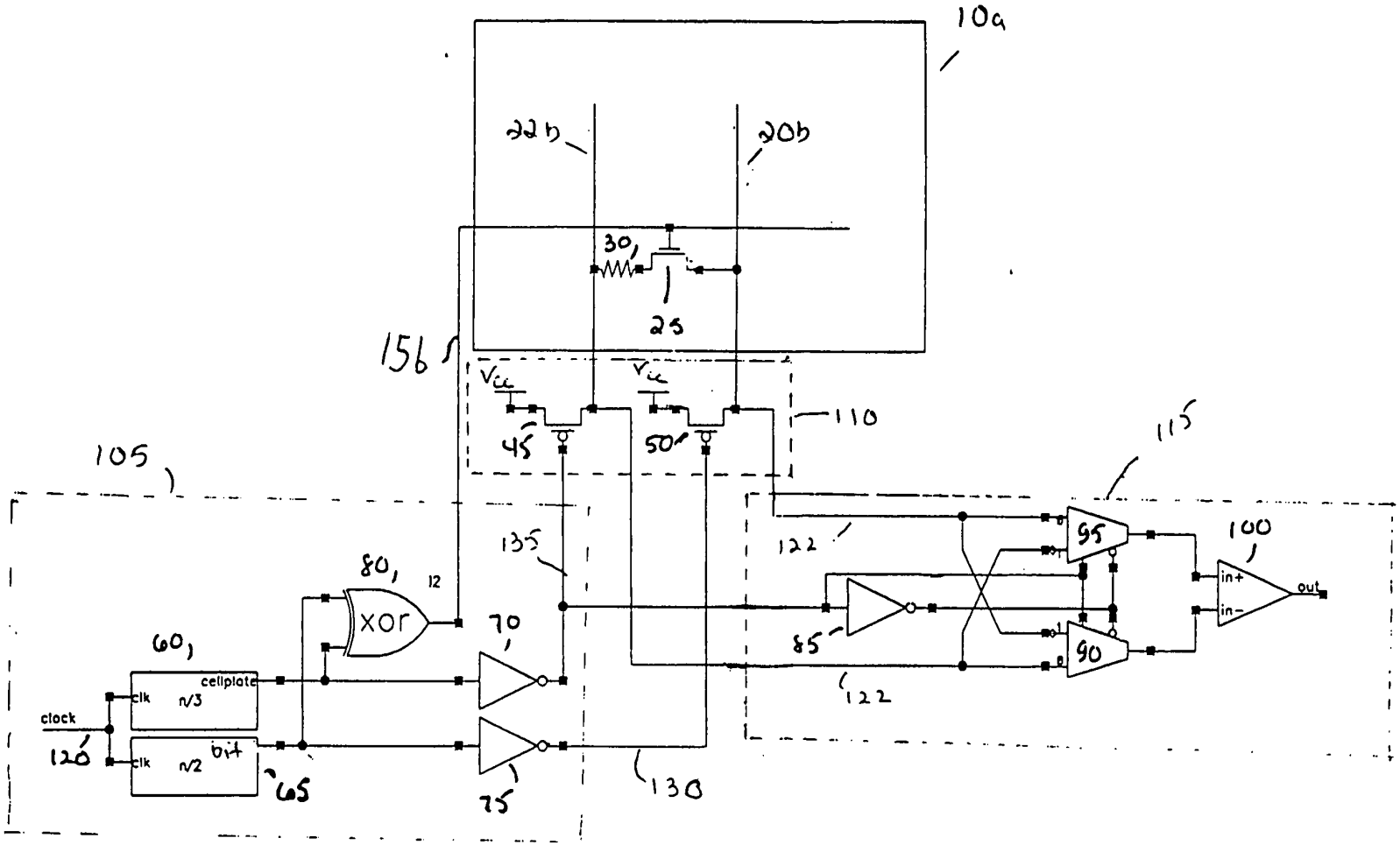
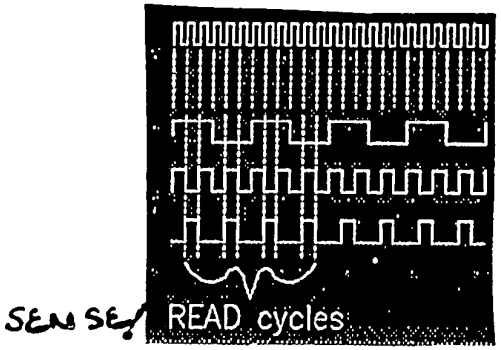

10a
22b
20b
30
25
156
Vcc
Vcc
110
45
50
105
115
135
122
95
100
80
12
XOR
70
85
90
in+
in-
out
60
cellplate
clk
n/3
clock
120
clk
n/2
bit
65
75
130
122

FIG. 2B



source clock signal 120

Signal 135

Signal 130

Signal on line 156

SENSE

FIG. 3

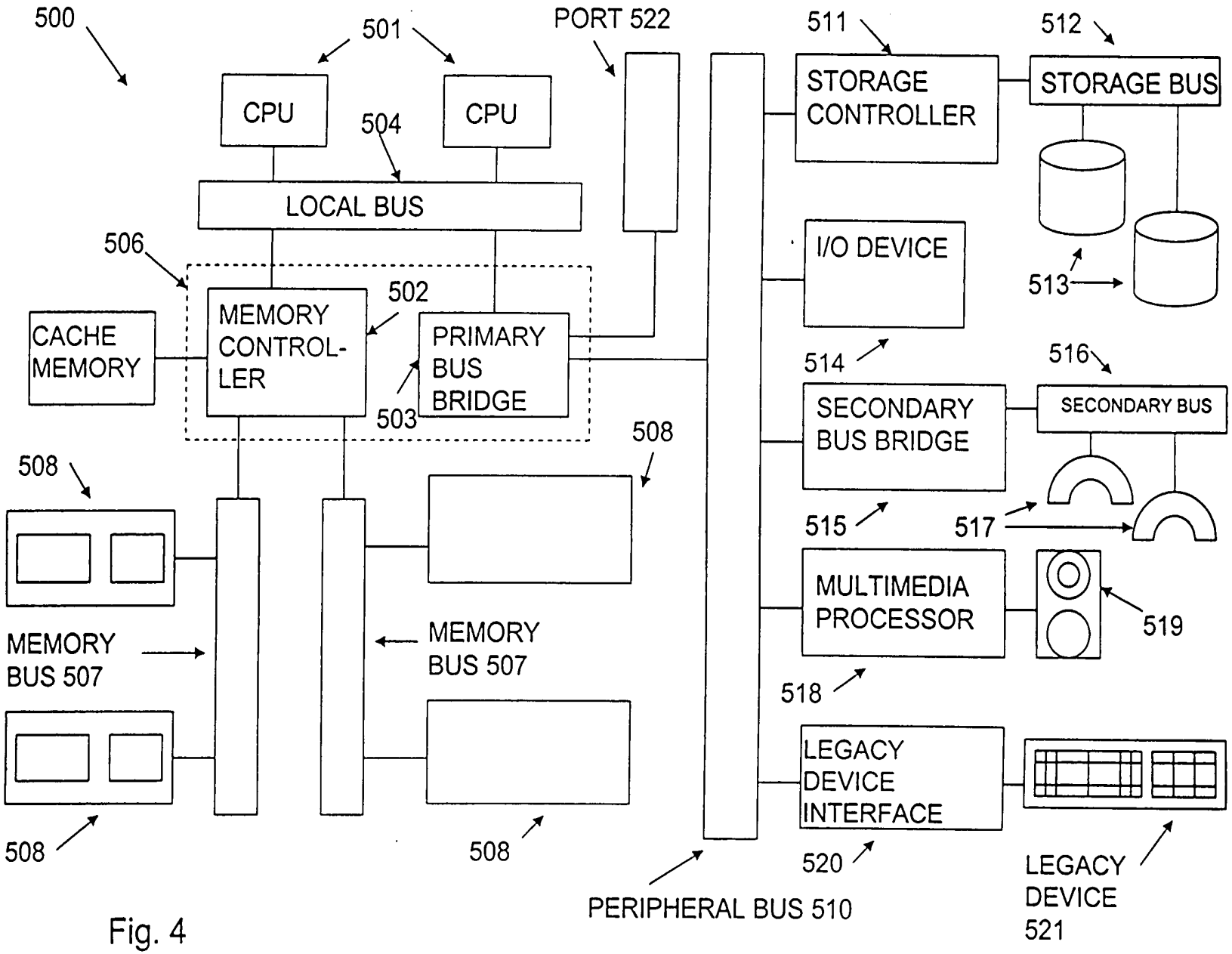

500
501
CPU
CPU
504
LOCAL BUS
506
502
MEMORY CONTROL-LER
CACHE MEMORY
PRIMARY BUS BRIDGE
503
PORT 522
508
508
MEMORY BUS 507
MEMORY BUS 507
508
508
PERIPHERAL BUS 510
511
STORAGE CONTROLLER
512
STORAGE BUS
513
I/O DEVICE
514
516
SECONDARY BUS BRIDGE
SECONDARY BUS
515
517
MULTIMEDIA PROCESSOR
519
518
LEGACY DEVICE INTERFACE
520
LEGACY DEVICE 521

Fig. 4